REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Upon entry of this Amendment, claims 1, 3, 5, 6, 9 will be pending in this application. Claim 9 has been added. Claims 2, 4, 7 and 8 are cancelled herein.

Election/ Restriction

The Applicants hereby elect to prosecute the invention of Group I, claims 1, 3, 5, 6 and 8. Claims 2, 4 and 7 are cancelled without prejudice to refiling them in a divisional application.

Drawings

As requested by the Examiner, the Applicants have amended Figures 13, 14, 15A-J, 16 and 17 and designated Figures 13, 14, 15A-J, 16 and 17 by the legend "Prior Art". Please see the enclosed drawing authorization request. Therefore, the Applicants respectfully request that the objection to the drawings be withdrawn.

Specification

The disclosure is objected to because of the informalities in the background of the invention for the use of the term "conventional". The Applicants have amended Figures 13, 14, 15A-J, 16 and 17 and designated the Figures by "Prior Art". Therefore the use of the term "conventional" when referring to these Figures has been clarified. With regard to page 25, line 28, the specification is correct it should read "Fig. 6".

Claim Objection

Claim 6 is objected to because of informalities. The Applicants have amended claim 6 to clarify the claim language. Therefore, The Applicants respectfully submit that the objection be withdrawn. Claim 8 has been cancelled. Therefore the objection is rendered moot.

Claim Rejection – 35 USC § 112

Claims 3, 6 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The Applicants have amended claims 3 to further clarify the intended meaning of the claim. Specifically, as indicated by the Examiner in page 4 and page 5, paragraph 11 of the Official Action, the phrase "polysilicon island" is further clarified to refer to "monocrystalline silicon islands". Claim 6 has also been amended to clarify the claim language. Specifically, the term "value" is deleted and replaced by the term "height". Therefore the terms "maximum" and "minimum" both refer to "height". Claim 8 has been cancelled. Therefore the objection is rendered moot.

Consequently, the Applicants respectfully submit that all pending claims are in full compliance with 35 USC §112.

Claim Rejection – 35 USC § 102 and 35 USC § 103

Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated Okonogi (US 5,420,064).

The Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites "A dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands mutually defined by a dielectrically separating oxide film on the surface of the wafer, wherein said dielectrically separated silicon islands comprise a high concentration impurity layer formed on the bottom of the islands and a low concentration impurity layer having an identical conductivity laminated on the high concentration impurity layer." In contrast, Okonogi is directed to a method of manufacturing a dielectric isolation substrate. In Figure 2 of Okonogi, the dielectrically separated wafer obtained by Okonogi's method is formed such that the single crystal silicon islands 11a are separated by polysilicon layer 14, silicon oxide layer 13 and n+ doped layer 12. Okonogi does not disclose or suggest a high concentration impurity layer formed on the bottom of the islands and/or a low concentration impurity layer having an identical conductivity laminated on the high concentration layer. In fact, layer 12 referred to, by the Examiner, as "the high concentration impurity layer" is merely an n+-type layer (cf., Col. 3, line 30-32). Okonogi does not disclose or suggest that layer 12 is a "high concentration impurity layer". Moreover, the Examiner contends that the low concentration impurity layer in Okonogi corresponds to the "remainder of 11a". However, Okonogi clearly indicates that layer 11a is "an island-like monocrystalline silicon film" (cf., Col. 3, line 10-11). The low concentration impurity layer of the present invention is laminated on the high concentration impurity layer (cf, Figure 1 of

the present invention). Consequently, Okonogi does not disclose or suggest a low concentration impurity layer.

Therefore, the Applicants respectfully submit that claim 1 is patentable and request that the §102 rejection be withdrawn.

With regard to claim 5, Okonogi does not disclose or suggest that "...a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat." In Okonogi the oxide layer 13, i.e., dielectrically separating layer, is not flat. To the contrary, the dielectric layer in Okonogi is "V-shaped" as clearly illustrated in Figures 2, 1E and 3E. In contrast, the present invention, as recited in claim 5, requires that the surface between two neighboring dielectrically separated silicon islands be flat (cf., for example, Figure 1, where dielectrically separating oxide film 14 is illustrated being flat at the separation between two neighboring silicon islands). Consequently, Okonogi does not disclose or suggest "...a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat."

Therefore, the Applicants respectfully submit that claim 5 is patentable and request that the §102 rejection be withdrawn.

Claims 3, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious from Okonogi (US 5,420,064).

The Applicants respectfully traverse these rejections for at least the following reasons.

Claim 3 recites, *inter alia*, "said polysilicon layer is formed by a seed polysilicon layer grown by a low temperature CVD method on the interface with said dielectrically separating oxide film and the polysilicon layer formed by a high temperature CVD method."

Specifically, the polysilicon layer used for separating the silicon islands is comprised of two layers, a low temperature polysilicon layer and a high temperature polysilicon layer. This two-layer structure makes the separating layer of the silicon islands homogenous, thus avoiding formation of voids between the polysilicon layer and the silicon oxide layer. Accordingly, Okonogi does not disclose or suggest a polysilicon layer comprised of a low temperature layer and a high temperature layer much less the characteristics of the layer avoiding formation of voids between the polysilicon layer and the oxide layer.

Claim 6 is dependent upon allowable claim 1. Therefore claim 6 is also allowable for at least the raison that it depends upon allowable claim 1. Furthermore, claim 6 recites, *inter alia*, "a flatness of the dielectrically separated silicon wafer is less than 0.2μm as the absolute

roughnesss between a maximum height and a minimum height." Specifically, the separating layer has a flatness of less than 0.2 μm. This allows the area of each silicon island to be enlarged resulting in suppression of defects that may occur during the manufacturing process. Accordingly, Okonogi does not disclose or suggest the dielectric separated silicon of the present invention as recited in claim 6.

Therefore, the Applicants respectfully submit that claims 3 and 6 are patentable and request that the §102 and §103 rejections be withdrawn.

Claim 8 has been cancelled herein. Therefore the §102 and §103 rejections are rendered moot.

Claim 9 has been newly added. Support for the claim language can be found throughout the specification and in particular on page 33, line 12 of the specification, where it is indicated "the flatness is below 0.2 μm". Claim 9 is dependent upon allowable claim 3. Therefore claim 9 is also allowable for at least the reason that it depends upon allowable claim 3.

CONCLUSION

In view of the foregoing, the claims are now in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Attached: Appendix

APPENDIX: VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The claims were amended as follows:

1. (Amended) A dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands mutually defined by a dielectrically separating oxide film on [the] a surface of the wafer, wherein said dielectrically separated silicon islands comprise:

a high concentration impurity layer formed on [the] a bottom of the islands; and

a low concentration impurity layer having an identical conductivity laminated on the high concentration impurity layer.

3. (Amended) A dielectrically separated wafer having a polysilicon layer and a plurality of [polysilicon island] monocrystalline silicon islands mutually separated by a dielectrically separating layer [formed] consisting of a silicon oxide film which is formed on [the] a surface of a polysilicon layer, wherein:

said polysilicon layer is formed by a seed polysilicon layer grown by a low temperature CVD method on [the] an interface with said dielectrically separating oxide film and [the] a polysilicon layer formed by a high temperature CVD method.

5. (Amended) A dielectrically separated wafer, having a plurality of dielectrically separated monocrystalline silicon islands insulated by a dielectrically separating oxide film on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat.

6. (Amended) A dielectrically separated silicon wafer according to claim 1, wherein, when this surface is measured by a stylus-profilometer, a flatness of the dielectrically separated silicon wafer is [for which the flatness of a surface between these the dielectrically separated silicon islands is] less than 0.2 μm as the absolute roughness between [the] a maximum [value] height and [the] a minimum [value] height.

End of Appendix